AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A surge protection device, comprising:

an insulator;

a gate electrode embedded in ~~an~~ said insulator;

a source electrode and a drain electrode on said insulator, ~~the~~ said source and drain electrodes respectively forming first and second capacitances with ~~the~~ said gate electrode; and

a semiconductor island on said insulator, ~~the~~ said island forming a channel region between said source and drain electrodes and forming a third capacitance with said gate electrode, ~~the~~ said third capacitance being smaller than either of said first and second capacitances,

said source and drain electrodes being adapted for connection to external circuitry for establishing a low-impedance path when ~~said~~ the external circuitry is subjected to a surge potential.

2. (Original) The surge protection device of claim 1, wherein said first and second capacitances are of equal value.

3. (Currently amended) A surge protection circuit, comprising:

a plurality of surge protection devices, each of said protection devices comprising:

an insulator;

a gate electrode embedded in ~~an~~ said insulator;

a source electrode and a drain electrode on said insulator, ~~the~~ said source and drain electrodes respectively forming first and second capacitances with ~~the~~ said gate

electrode; and

a semiconductor island on said insulator, ~~the~~ said island forming a channel region between said source and drain electrodes and forming a third capacitance with said gate electrode, ~~the~~ said third capacitance being smaller than either of said first and second capacitances,

~~the~~ said source and drain electrodes of each of said surge protection devices being respectively connected to the drain and source electrodes of adjacent ones of said plurality of surge protection devices and ~~further~~ adapted to be connected to pad electrodes of external circuitry for establishing connections with said adjacent surge protection devices when one of ~~said~~ the pad electrodes is subjected to a surge potential.

4. (Original) The surge protection circuit of claim 3, wherein said first and second capacitances of each of said surge protection devices are of equal value.

5. (Currently amended) The surge protection circuit of claim 3, further comprising:

a second plurality of surge protection devices identical in structure to said plurality of surge protection devices,

the source-drain paths of ~~the~~ said second plurality of surge protection devices being respectively connected to ~~said~~ the pad electrodes via respective lines for establishing a low-impedance path to ground.

6. (Currently amended) The surge protection circuit of claim 3, further comprising:

a ~~second~~ first additional surge protection device identical in structure to said plurality of surge protection devices and connected between a first one of said plurality of surge

protection devices and ground; and

a ~~third~~ second additional surge protection device identical in structure to said plurality of surge protection devices and connected between a second one of said plurality of surge protection devices and ground.

7. (Currently amended) The surge protection circuit of claim 6, further comprising a second plurality of surge protection devices identical in structure to said plurality of surge protection devices, the source-drain paths of ~~the~~ said second plurality of surge protection devices being respectively connected to ~~said~~ the pad electrodes via respective lines for establishing a low-impedance path to ground.

8. (Currently amended) A surge protection circuit, comprising:

a plurality of surge protection devices, each of said protection devices comprising:

an insulator;

a gate electrode embedded in ~~an~~ said insulator;

a source electrode and a drain electrode on said insulator, ~~the~~ said source and drain electrodes respectively forming first and second capacitances with ~~the~~ said gate electrode; and

a semiconductor island on said insulator, ~~the~~ said island forming a channel region between said source and drain electrodes and forming a third capacitance with said gate electrode, ~~the~~ said third capacitance being smaller than either of said first and second capacitances,

~~the~~ said source and drain electrodes of each of said surge protection devices being adapted to be connected in series to external circuitry for establishing a low-impedance path

to ground when the external circuitry is subjected to a surge potential.

9. (Original) The surge protection circuit of claim 8, wherein said first and second capacitances of each of said surge protection devices are of equal value.

10. (Currently amended) A surge protection circuit for a semiconductor display panel, ~~which includes~~ said circuit comprising:

a first plurality of pad electrodes;

a plurality of vertical signal lines connected respectively to said first plurality of pad electrodes;

a second plurality of pad electrodes; ~~and~~

a plurality of horizontal signal lines intersecting said vertical signal lines, ~~the~~ said horizontal signal lines being connected respectively to said second plurality of pad ~~electrodes,~~ electrodes; and

~~the surge protection circuit comprising~~ a plurality of floating-gate field effect transistors, each having a channel capacitance and including a floating gate electrode, a source electrode and a drain electrode, ~~the~~ said source and drain electrodes of each of said transistors being respectively connected to the drain and source electrodes of adjacent ones of said plurality of floating-gate transistors and further connected to respective ones of said first plurality of pad electrodes, each of said transistors being responsive to the respective pad electrode, or to the vertical signal line connected to the respective pad electrode, being subjected to a surge potential for ~~establishing~~ developing a voltage on said channel capacitance sufficient to turn on said floating-gate field effect transistor and establish connections with said adjacent floating-gate transistors. ~~when one of said first plurality of pad electrodes or one of said plurality of vertical signal lines is subjected to a surge potential.~~

11. (Currently amended) A ~~The~~ surge protection circuit ~~of claim 10,~~ for a semiconductor display panel, said circuit comprising:

a first plurality of pad electrodes;

a plurality of vertical signal lines connected respectively to said first plurality of pad electrodes;

a second plurality of pad electrodes;

a plurality of horizontal signal lines intersecting said vertical signal lines, the horizontal signal lines being connected respectively to said second plurality of pad electrodes; and

a plurality of floating-gate field effect transistors, each including an insulator, a floating gate electrode, a source electrode and a drain electrode, said source and drain electrodes of each of said transistors being respectively connected to the drain and source electrodes of adjacent ones of said plurality of floating-gate transistors and further connected to respective ones of said first plurality of pad electrodes for establishing connections with said adjacent floating-gate transistors when the respective pad electrode, or the vertical signal line connected to the respective pad electrode, is subjected to a surge potential,

wherein in each transistor said ~~the~~ floating gate electrode ~~of each of said floating gate field effect transistors~~ is embedded in ~~an~~ said insulator, ~~and~~ said source electrode and said drain electrode are formed on said insulator so that ~~the~~ said source and drain electrodes respectively form first and second capacitances with ~~the~~ said floating gate electrode, and a semiconductor island is provided on said insulator to form a channel between said source and drain electrodes and to form a third capacitance with said gate electrode, ~~the~~ said third capacitance being smaller than either of said first and second capacitances.

12. (Currently amended) The surge protection circuit of claim ~~10~~ 11, wherein said first and second capacitances of each of said floating-gate transistors are of equal value.

13. (Currently amended) The surge protection circuit of claim 10, further comprising a second plurality of floating-gate transistors, ~~the~~ said source-drain paths of ~~the~~ said second plurality of floating-gate transistors being respectively connected to said first plurality of pad electrodes via respective lines for establishing a low-impedance path to ground.

14. (Currently amended) The surge protection circuit of claim 10, further comprising:

a ~~second~~ first additional floating-gate transistor connected between a first one of said plurality of floating-gate transistors and ground; and

a ~~third~~ second additional floating-gate transistor connected between a second one of said plurality of floating-gate transistors and ground.

15. (Currently amended) The surge protection circuit of claim 14, further comprising a second plurality of floating-gate transistors, the source-drain paths of ~~the~~ said second plurality of floating-gate transistors being respectively connected to said first plurality of pad electrodes via said vertical signal lines for establishing a low-impedance path to ground.

16. (Currently amended) A surge protection circuit for a semiconductor display panel, ~~which includes~~ comprising:

a first plurality of pad electrodes;

a plurality of vertical signal lines connected respectively to said first plurality of pad electrodes;

a second plurality of pad electrodes; ~~and~~

a plurality of horizontal signal lines intersecting said vertical signal lines, the horizontal signal lines being connected respectively to said second plurality of pad electrodes, and

~~the surge protection circuit comprising~~ a plurality of floating-gate field effect transistors, each having a channel capacitance and including a floating gate electrode, a source electrode and a drain electrode, ~~the~~ said source and drain electrodes of each of said transistors being respectively connected to said vertical signal lines, each of said transistors being responsive to the respective vertical signal line, or the pad electrode connected to the respective vertical signal line, being subjected to a surge potential for ~~establishing~~ developing a voltage on said channel capacitance sufficient to turn on said floating-gate field effect transistor and establish a low-impedance path to ground. ~~when one of said first plurality of pad electrodes or one of said plurality of vertical signal lines is subjected to a surge potential.~~

17. (Currently amended) A ~~The~~ surge protection circuit ~~of claim 16,~~ for a semiconductor display panel, said circuit comprising:

a first plurality of pad electrodes;

a plurality of vertical signal lines connected respectively to said first plurality of pad electrodes;

a second plurality of pad electrodes;

a plurality of horizontal signal lines intersecting said vertical signal lines, the horizontal signal lines being connected respectively to said second plurality of pad electrodes, and

a plurality of floating-gate field effect transistors, each including an insulator, a floating gate electrode, a source electrode and a drain electrode, said source and drain electrodes of each of said transistors being respectively connected to said vertical signal lines for establishing a low-impedance path to ground when the respective vertical signal line, or the pad electrode connected to the respective vertical signal line, is subjected to a surge potential,

wherein in each transistor said ~~the~~ floating gate electrode ~~of each of said floating-gate field effect transistors~~ is embedded in ~~an~~ said insulator, and said source electrode and said drain electrode are formed on said insulator so that ~~the~~ said source and drain electrodes respectively form first and second capacitances with ~~the~~ said floating gate electrode, and a semiconductor island is provided on said insulator to form a channel between said source and drain electrodes and to form a third capacitance with said gate electrode, the third capacitance being smaller than either of said first and second capacitances.

18. (Original) The surge protection circuit of claim 17, wherein said first and second capacitances of each of said floating-gate transistors are of equal value.

19. (New) A surge protection device, comprising:

a gate electrode;

a source electrode forming a first capacitance with said gate electrode;

a drain electrode forming a second capacitance with said gate electrode; and

a channel region between said source and drain electrodes and forming a third capacitance with said gate electrode, said third capacitance being smaller than either of said first and second capacitances,

said source and drain electrodes being adapted for connection to external circuitry for establishing a low-impedance path when the external circuitry is subjected to a surge potential.

20. (New) A surge protection circuit, comprising:

a plurality of surge protection devices, each of said protection devices comprising:

a gate electrode;

a source electrode forming a first capacitance with said gate electrode;

a drain electrode forming a second capacitance with said gate electrode; and

a channel region between said source and drain electrodes and forming a third capacitance with said gate electrode, said third capacitance being smaller than either of said first and second capacitances,

said source and drain electrodes of each of said surge protection devices being respectively connected to the drain and source electrodes of adjacent ones of said plurality of surge protection devices and adapted to be connected to pad electrodes of external circuitry for establishing connections with said adjacent surge protection devices when one of the pad electrodes is subjected to a surge potential.

21. (New) A surge protection circuit, comprising:

a plurality of surge protection devices, each of said protection devices comprising:

a gate electrode;

a source electrode forming a first capacitance with said gate electrode;

a drain electrode forming a second capacitance with said gate electrode; and

a semiconductor island forming a channel region between said source and drain electrodes and forming a third capacitance with said gate electrode, said third capacitance being smaller than either of said first and second capacitances,

said source and drain electrodes of each of said surge protection devices being adapted to be connected in series to external circuitry for establishing a low-impedance path to ground when the external circuitry is subjected to a surge potential.

22. (New) A surge protection circuit for a semiconductor display panel, said circuit comprising:

a plurality of vertical signal lines;

a plurality of horizontal signal lines intersecting said vertical signal lines; and

a plurality of floating-gate field effect transistors, each having a channel capacitance and including a floating gate electrode, a source electrode and a drain electrode, said source and drain electrodes of each of said transistors being respectively connected to the drain and source electrodes of adjacent ones of said plurality of floating-gate transistors and adapted to be connected to respective pad electrodes so as to be responsive to the respective pad electrode being subjected to a surge potential for developing a voltage on said channel capacitance sufficient to turn on said floating-gate field effect transistor and establish connections with said adjacent floating-gate transistors.

23. (New) A surge protection circuit for a semiconductor display panel, comprising:

a plurality of vertical signal lines;

a plurality of horizontal signal lines intersecting said vertical signal lines; and

a plurality of floating-gate field effect transistors, each having a channel capacitance and including a floating gate electrode, a source electrode and a drain electrode, said source and drain electrodes of each of said transistors being respectively connected to said vertical signal lines, each of said transistors being responsive to the respective vertical signal line being subjected to a surge potential for developing a voltage on said channel capacitance sufficient to turn on said floating-gate field effect transistor and establish a low-impedance path to ground.